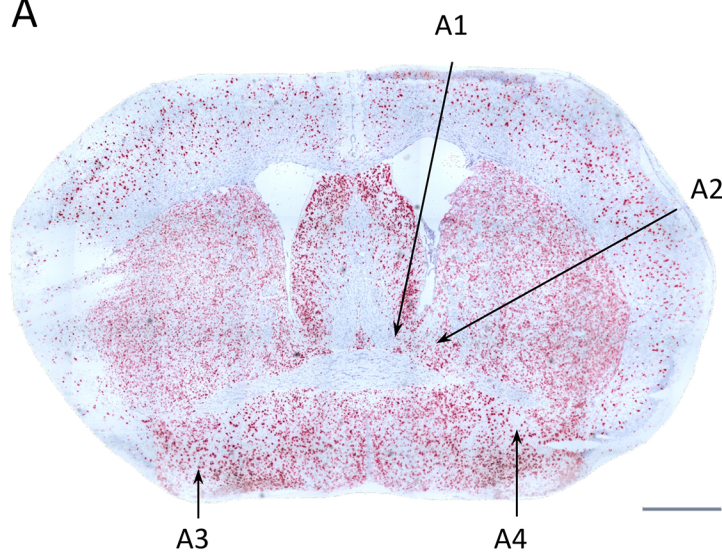
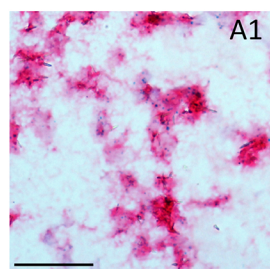


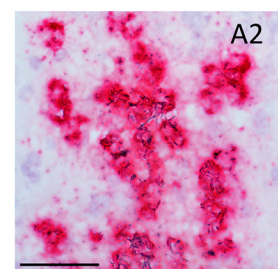
A



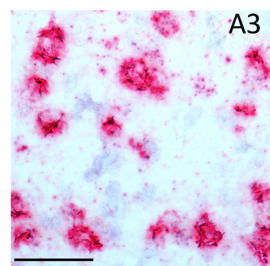
Slc32a1 *Vipr2*



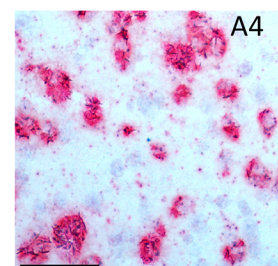
BSTam



BSTov

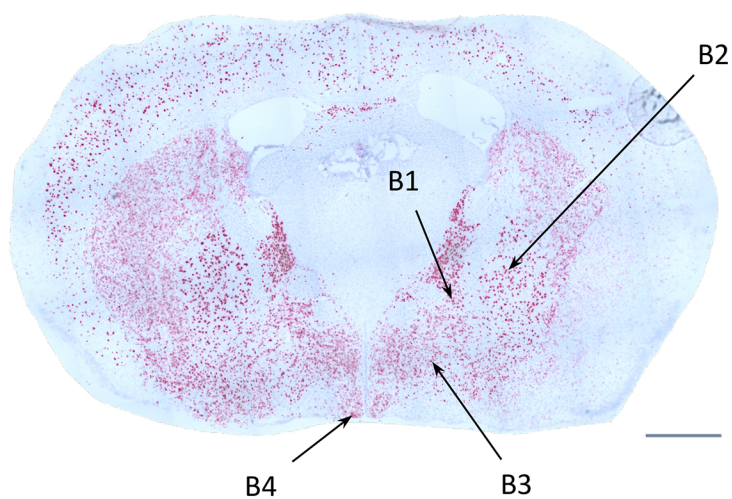


MA

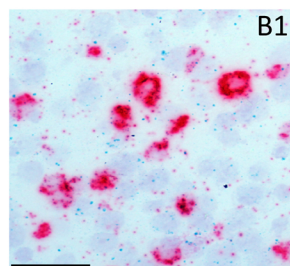


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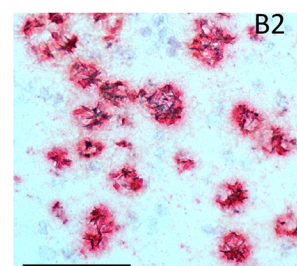
B



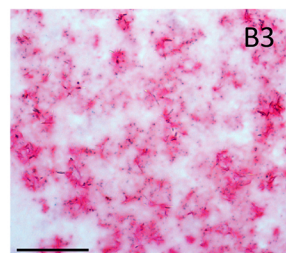
Slc32a1 *Vipr2*



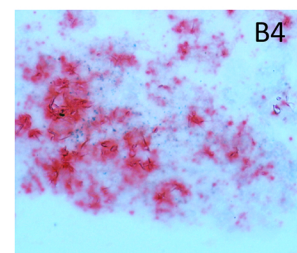
BSTpr



GPe

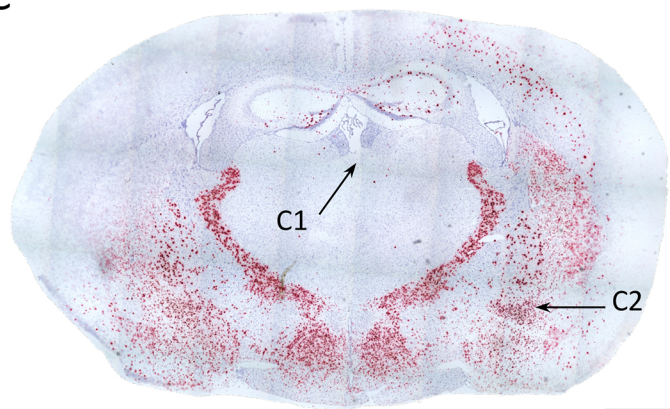
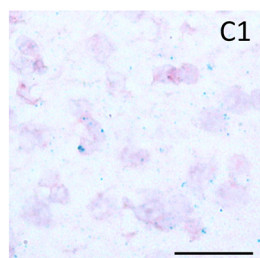


MPO

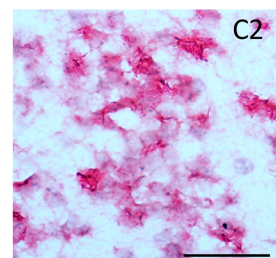


SCH

C

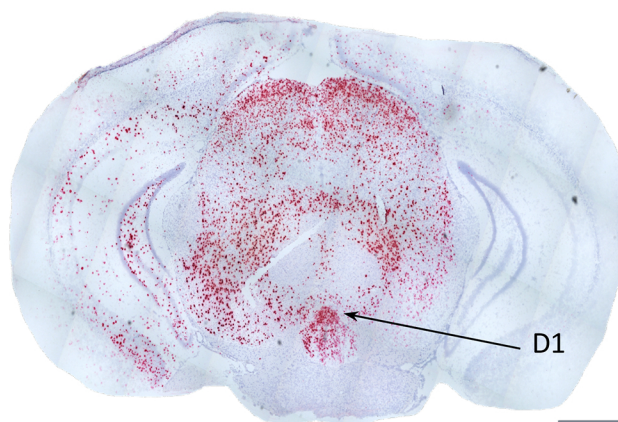
*Slc32a1 Vipr2*

PVT



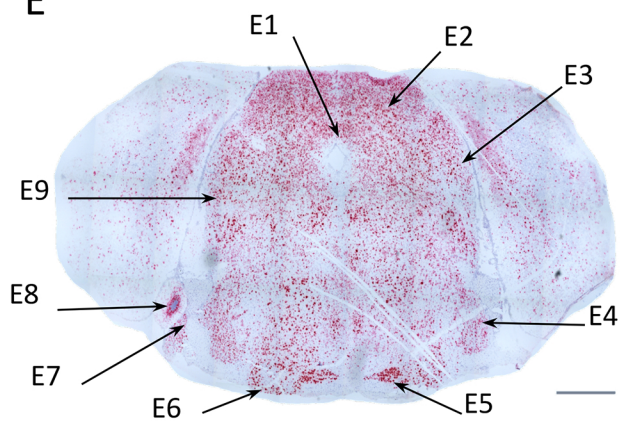
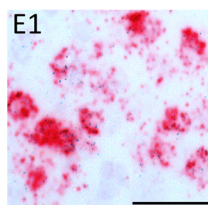
CEAc

D

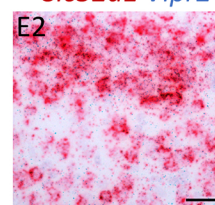
*Slc32a1 Vipr2*

IPN

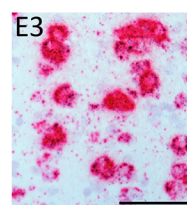
E

*Slc32a1 Vipr2*

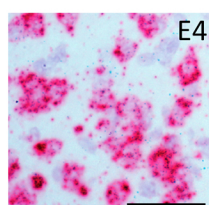
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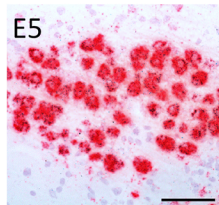
SC s>m



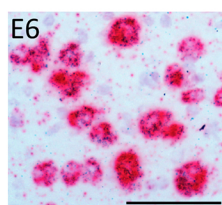
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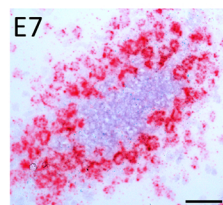
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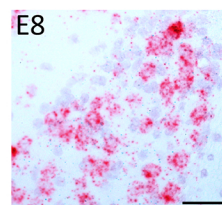
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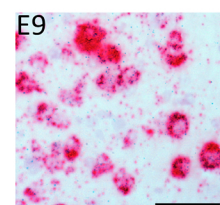
SOC



FL, Cb

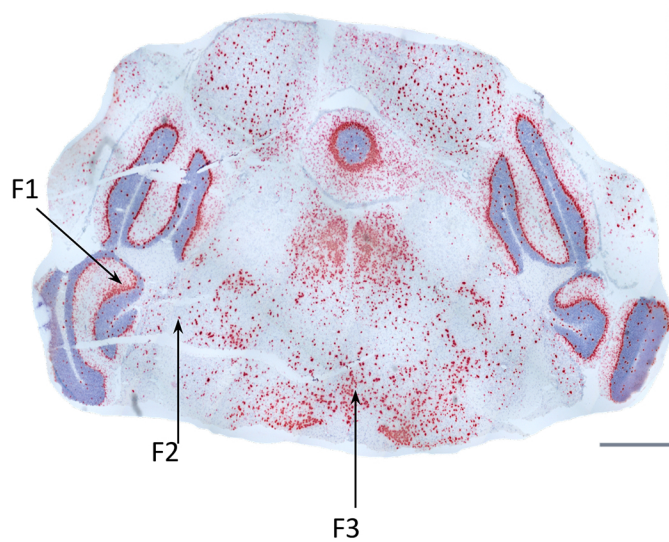


VCO

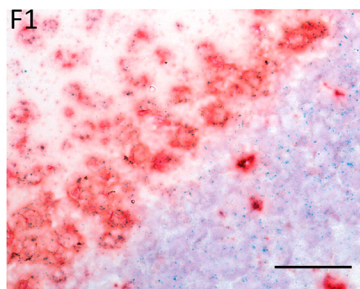


IC

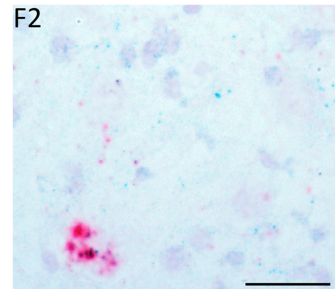
F

*Slc32a1 Vipr2*

F1



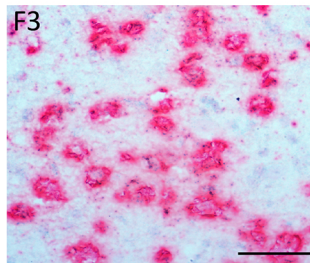
F2



PFL

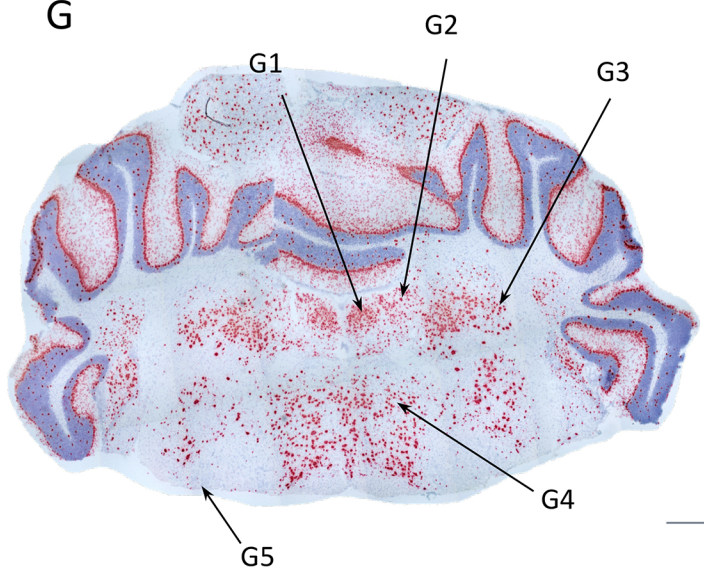
V

F3

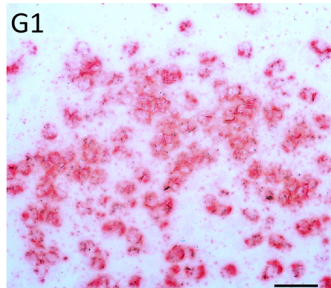


RM

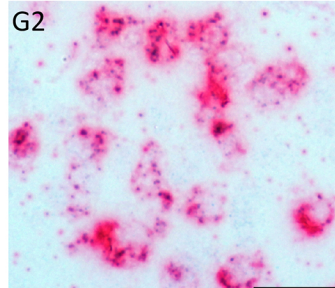
G

*Slc32a1 Vipr2*

G1



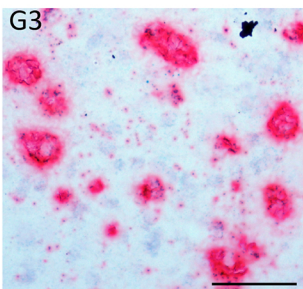
G2



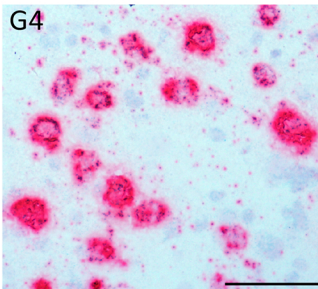
DTN

PCG

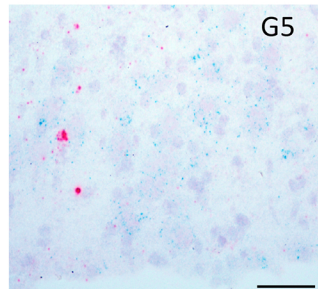
G3



G4



G5



VNC

GRN

VII